reading the program from the memory;

detecting the pseudo instruction;

prefetching the instruction or data from the memory in accordance with the at least one instruction address or the data address; and

storing the prefetched instruction or data in a buffer.

8. (Amended) A microcontroller, comprising:

a buffer, connected to a memory, for storing instructions and data of a program prefetched from the memory, wherein the program includes a pseudo instruction, at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, and at least one instruction address or data address being part of he pseudo instruction, and wherein the pseudo instruction is not executed;

an instruction execution unit, connected to the buffer, for receiving the instruction and data from the buffer and executing a predetermined processing operation using the instruction and data;

a pseudo instruction detection unit, connected to the memory, for detecting the pseudo instruction included in the program prefetched from the memory; and

an address control unit, connected to the external memory and the pseudo instruction detection unit, for prefetching the instruction or data in accordance with at least one instruction address or data address when the pseudo instruction is detected.

14. (Amended) A device for detecting a pseudo instruction present before a specific instruction, wherein the pseudo instruction includes an opcode and an operand, and wherein the pseudo instruction is not executed, the device comprising:

a detecting circuit, connected to a data line, for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction; and

a detection timing circuit, connected to the detecting circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for invalidating the opcode detection operation during an operand transfer period.

15. (Amended) A recording medium having a program stored thereon, wherein the program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, wherein the pseudo instruction is not executed, and wherein the at least one instruction address or data address is part of the pseudo instruction.

16. (Amended) A microcontroller connected to a memory which stores instructions and data, the microcontroller comprising:

an instruction execution unit for reading instructions and data from the memory and processing the read instructions; and

a prefetch circuit unit that receives instructions and data read from the memory in response to a fetch signal, and detects pseudo instructions included in the instructions and data, wherein a pseudo instruction precedes a branch instruction and indicates the existence of the branch instruction, and wherein the pseudo instruction is not executed;

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wherein the prefetch circuit unit includes,

a prefetch buffer connected between the instruction execution unit and the memory for temporarily storing instructions and data being transferred from the memory to the instruction execution unit,

a bus interconnecting the prefetch buffer and the memory,

a pseudo instruction detection unit connected to the bus for detecting pseudo instructions among he instructions and data being transferred from the memory to the prefetch buffer,

a holding circuit, connected to the bus and to the pseudo instruction detecting unit, for storing operands of the pseudo instruction,

a pseudo instruction buffer for temporarily storing instructions and data fetched from a location in the memory which is pointed to by the branch instruction following the pseudo instruction,

an address control unit for generating the fetch signal and for generating a memory address which points to the address of a next word to be read from the memory, and wherein when the pseudo instruction detection unit detects a pseudo instruction, the instructions and data pointed to by the pseudo instruction are fetched

from the memory by the address control unit and stored in the pseudo instruction buffer so that when the branch instruction following the pseudo instruction is processed by the instruction execution unit, if the branch is taken, the instructions and data pointed to by the branch instruction have been prefetched and stored in the pseudo instruction buffer.

Please add new claims 19-23, as follows:

19. (New) A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, wherein the pseudo instruction has at least one instruction address or data address that is stored before the at least one instruction is fetched, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction;

prefetching the instruction or data from the memory in accordance with the at least one instruction address or the data address; and

storing the prefetched instruction or data in a buffer.

20. (New) A microcontroller, comprising:

a buffer, connected to a memory, for storing instructions and data of a program prefetched from the memory, wherein the program includes a pseudo instruction, at

least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, wherein the pseudo instruction has at least one instruction address or data address that is stored before the at least one instruction is fetched;

an instruction execution unit, connected to the buffer, for receiving the instruction and data from the buffer and executing a predetermined processing operation using the instruction and data;

a pseudo instruction detection unit, connected to the memory, for detecting the pseudo instruction included in the program prefetched from the memory; and

an address control unit, connected to the external memory and the pseudo instruction detection unit, for prefetching the instruction or data in accordance with the at least one instruction address or data address when the pseudo instruction is detected.

21. (New) A device for detecting a pseudo instruction preset before a specific instruction, wherein the pseudo instruction includes an opcode and an operand, wherein the operand includes at least one instruction address or data address that is stored before the specific instruction is fetched, the device comprising:

a detection circuit, connected to a data line, for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction; and

a detection timing circuit, connected to the detection circuit, for calculating instruction length or a number of operands of the pseudo instruction from the opcode and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for invalidating the opcode detection operation during an operand transfer period.

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cont.

22. (New) A recording medium having a program stored thereon, wherein the program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, a pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, wherein the pseudo instruction has at least one instruction address or data address that is stored before the at least one instruction is fetched.

23. (New) A microcontroller connected to a memory which stores instructions and data, the microcontroller comprising:

an instruction execution unit for reading instructions and data from the memory and processing the read instructions; and

a prefetch circuit unit that receives instructions and data read from the memory in response to a fetch signal, and detects pseudo instructions included in the instructions and data, wherein a pseudo instruction precedes a branch instruction and indicates the existence of the branch instruction;

wherein the prefetch circuit unit includes,

a prefetch buffer connected between the instruction execution unit and the memory for temporarily storing instructions and data being transferred from the memory to the instruction execution unit,

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a bus interconnecting the prefetch buffer and the memory,

a pseudo instruction detection unit connected to the bus for detecting pseudo instructions among the instructions and data being transferred from the memory to the prefetch buffer,

a holding circuit, connected to the bus and to the pseudo instruction detection unit, for storing operands of the pseudo instruction, wherein the operand includes at least one instruction address or data address that is stored before at least one of the instructions is fetched,

a pseudo instruction buffer for temporarily storing instructions and data fetched from a location in the memory which is pointed to by the branch instruction following the pseudo instruction, and

an address control unit for generating the fetch signal and for generating a memory address which points to the address of a next word to be read from the memory, and wherein when the pseudo instruction detection unit detects a pseudo instruction, the instructions and data pointed to by the pseudo instruction are fetched from the memory by the address control unit and stored in the pseudo instruction buffer so that when the branch instruction following the pseudo instruction is processed by the instruction execution unit, if the branch is taken, the instructions and data pointed to by the branch instruction have been prefetched and stored in the pseudo instruction buffer.